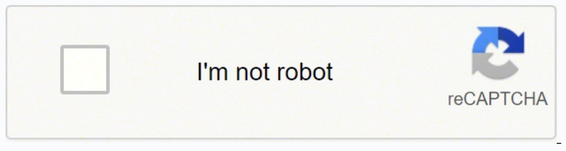

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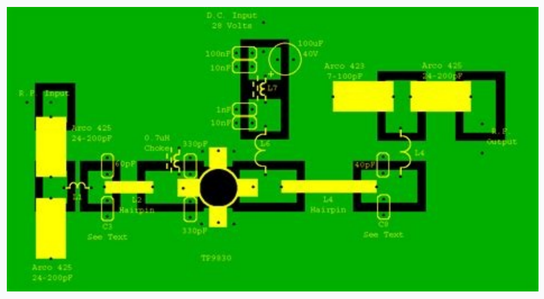
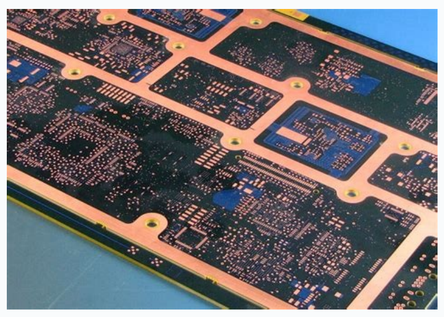
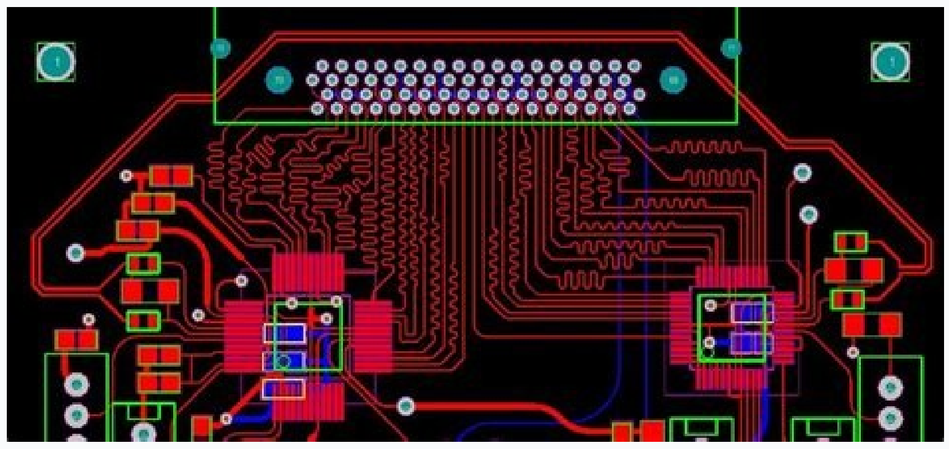
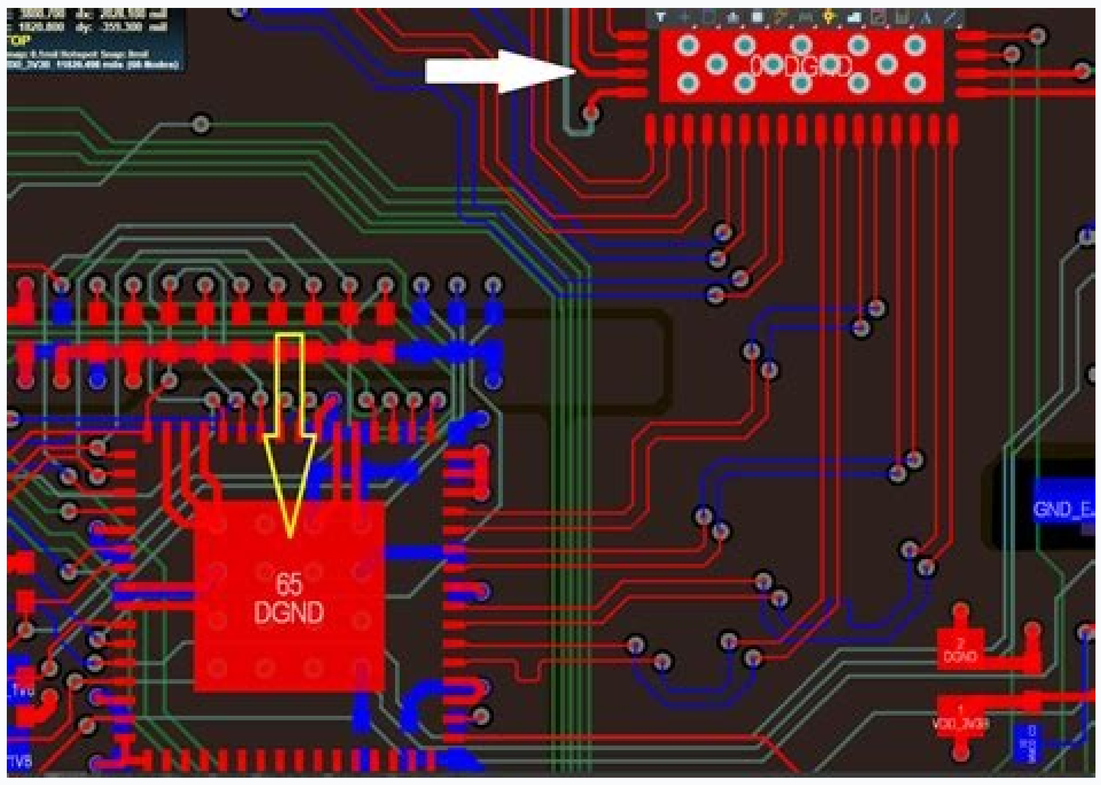
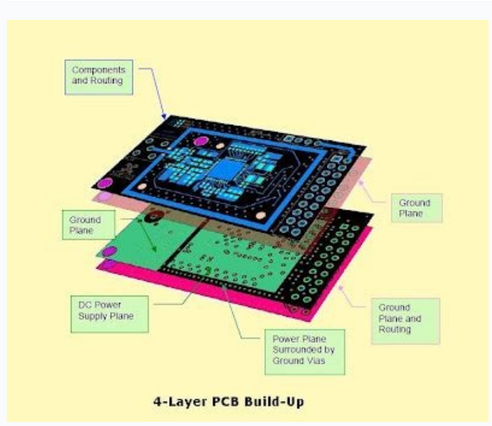
Rf pcb layout design guidelines











Rf design guidelines pcb layout and circuit optimization.

Usually this configuration requires a little more PCB area. The maximum number of roads that can be accommodated by other layout considerations should be used. In this configuration, the pathways that connect the VCC pad in the upper layer to the internal power plane (layer) prevent, in a pow © the return of the AC earth current, forcing a longer return path with the resulting higher parasitic inductance. For grounded components (such as power decoupling capacitors), the recommended practice is © use at least two earthing pathways for each component (Figure 12). In this alternative configuration, the return trajectories AC to earth are not blocked by the pathways of the power plane. This configuration requires more PCB area. AtravÃ © s of terrestrial "islands" can be used for groups of components bound by derivation. Table 2. Figure 4. The use of at least two grounding pathways for each component reduces the effect of parasitic inductance. Offset suspended stripe line. Whenever possible, signal lines carrying high power levels shall be kept away from all other lines. It is recommended to use seals on both sides of a coplanar waveguide. Esta fÃ³rmula Ã © independent of the dielÃ constant © ctrica, e estÃ¡ subjeta Ã restriÃ§Ã£o que w/h Ã¢Â¥ 0,25. It is recommended to use "fences" on both sides of a coplanar waveguide, as shown in Figure 5. Actual capacitors have limited effective frequency ranges due to their self-resonant frequency (SRF). This medium consists of a central conductor with ground planes on both sides and below (Figure 4). TUTORIALS 5100 By: Michael Bailey Abstract: This application note provides guidelines and suggestions for the design and layout of the RF Printed Circuit Board (PCB), including some discussions on mixed signal applications. Figure 7. This any characteristic impedance changes that move through © s of the curve. TambÃ © m describes curves of transmission lines and corner compensation, and layer changes to transmission lines. © all bÃ¡sicos, bÃ¡sicos, In Figure 10 and Figure 11. Consult our wireless and RF product page for more information. The example below shows an array of 5 Âƒ-5 of holes through the central plane (in the component layer) directly under the IC RF (Figure 13). When broadband dissociation is required, the standard pratic is to use several growing capacitors (capacitance), all connected in parallel. When a curve curve is not possible, the transmission line can undergo a straight angle curve. Figure 5. The main consideration with the decoupling of the offer is that the DC supply connections must be electrically defined as AC grounding. Incorrect layer assignment: There are signs of signal between the virtue layer and the rearing path of the ground layer. ©, Maxim Integrated Products, Inc. For Striplines and Offset Striplines, Solo Plans above and below the central conductor are required. Suspended Stripline This line consists of a fixed width routing in an internal layer, with soil plans are above and below the central conductor. Pair Preme -Prog (3.8) 6 (0.152) 25 (0.635) 6 (0.152) 50.6 Stripline FR4 (4,5) 12 (0.305) 3.7 (0.094) N / A 50.0 Offset Stripline PrePreg (3.9) 6 (0.152) upper, 10 (0.254) lower 4.8 (0.122) N / A 50.1 Coplanar WG PrePrg (3.8) 6 (0.152) 14 (0.35) 20 (0.55) 49.7 transmission line cables and corner compensation when transmission lines are required to bend (direction change) due to routing constraints use a bending radius that is at least 3 times the width of the central conductor. Above the SRF, the capacitor is inductive and therefore will not execute the function of decoupling or deviation. The driver can be located halfway between ground plans (Figure 2), or can be compensated (Figure 3). These parasitic inductions can be caused by layout options or component orientation, such as the guidance of a of decoupling capacitor. The material provides orientation \ "best practical \" and should be used in conjunction with all all fo selfmaxE .8 erugif .11 erugif . su tcatnoc ,tnetnoc siht ypoc ot stseuqer roF . enalp dnuorg dengissa eht ot BCP eht hguorht stnerruc nruter FR dna CD yrrac lliw enalp dnuorg sihT .6 erugif . sreyal langis eht ot delpuoc eb nac esion enil saiB .1 elbaT . tnemerusaem tcerid yb deziretcarahc eb tsum semitemos tub ,rerutcafunam eht morf elbaliava si FRS ehT . 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I'll tell you what. elbacilppa sa stes lairetam dna ,srerutcafunam BCP ,stnenopmoc ralucitrap ot ylppa yam taht seniledіug gnirutcafunam dna ngised od roirefni uo roirepus(etnenopmoc od adamac an odil³Ãs arret ed onalp mu reuqer IC sod airoiam A .lanis ed sahnil sartuo e samix³Ãrp FR ed sahnil ertne otnemalosi rohlem mu ecenrof ranalpoc adno ed aiug mU .dnuor adamac onretni rg on ranroter ed setna olos od odal o arap oivsed ed roticpac od s©Ãvarta assap CCV onip o arap odniulf CA etnerroc reuqlauQ .sadidnetse saicn¢Ãtsid arap edadimixorp atiertse me sadahnimacne res meved o£Ãn e ,levÃssop setnatsid siam o saditnam res meved sahnil sA :FR ed o£Ãssimsnart ed sahniL :savitneverp sadidem e sotnemalpoca siaicnetop ed solpmexe snuglA .sv soig¡Ãtseretni ,.e.i(acifÃcepse edadilanoicnuf aus a e ,FR CI od lanoicarepo aicnªÃuqerf ed axiaf ad edneped seroticapac somitlºÃ setsed rolav O .sadarapes sa-odnetnam arret ed onalp mu ret meved sadarapes sadamac me mazurc es euq sahniL .olos oa etnemavisulcxe sodÃubirta res meved sam ,aicnªÃtop ed uo o£Ã§Âazilanis ed seder a sodÃubirta uo sodahlitrap res meved o£Ãn sonalp setsE .BCP od s©Ãvarta lanis ed sahnil sartuo e FR ed odazurc otnemalpoca o rative a maduja m©Ãbmat saiv sA .)9 arugiF(o£Ã§Ãatnemila ed seµÃxenoc sair¡Âv revit etnenopmoc mu es ,o£Ã§Ãatnemila ed sator sa arap "alertse" o£Ã§Ãarugifnoc amu rasu ©Ã mumoc acit¡Ârp amU .ohnepmesed otla ed o£Ãssimsnart ed sahnil rigixe otejorp o es ocit©Ângamortele rodalumis mu odnasu adaledom res eved avruc a ,aterroc o£Ã§Ãasnepmoc Ã otnauq azetrecni amugla revuoh eS .oxiaba odartsom ©Ã olpmexe mU .)adavruc o£Ãn(ralugna avruc amu rerfos edop o£Ãssimsnart ed ahnil a ,levÃssop ©Ã o£Ãn laudarg avruc amu euq me sosac soN .sahnil ertne otnemalosi etnelecxe ecenrof odarreta ranalpoc adno ed aiug O .sadanoicaler saiv e ssapyb ed roticpac o arap latot adagep ronem a atneserpa o£Ã§Ãarugifnoc assE .01 arugiF a§Ãnerefi D 0,05)805,0(02)452,0(01 3,05 A/N)292,0(5,11)251,0(6)8,3(gerperP pirtsorciM aicn¢ÂdepmI acitsÃretcaraC paG)mm(slim me lartnec rotudnoC)mm(slim me aicn¢Âdepmi ed soiem sod adamac ad acirt©Âleid arussepsE directly below the component. SRF component capacitance package useful frequency ranges Useful* useful* frequency range Range 20pF 0402 2.5GHz 800MHz to 2.5GHz Very High Range 100pF 0402 800MHz 250MHz to 800MHz High Range 1000pF 0402 250MHz 50MHz to 250MHz Midrange 1ÃµÂF 0402 60MHz 100kHz to 60MHz Low Range 10ÃµÂF 0603 600kHz 10kHz to 600kHz *Low end of useful frequency range defined as less than 5Ã©Â of capacitive reactance. However, caution should be used when entering the dielectric constant of the layers. Partial ground planes on a layer, sometimes required by design constraints, must underlie all RF components and transmission lines. This helps prevent accrual of parasitic ground inductance due to ground-current return paths. A standard compensation method is the angled miter, as illustrated below. Microstrip This type of transmission line consists of fixed-width metal routing (the conductor), along with a solid unbroken ground plane located directly underneath (on the adjacent layer). Figure 1. Similar methods can be employed for other transmission lines. Guidelines for these transmission lines include discussions relating to the microstrip, suspended stripline, coplanar waveguide (grounded), and characteristic impedance. Coupling between parallel microstrip lines will increase with decreasing separation and increasing parallel routing distance. VCC/Power Lines: These should be routed on a dedicated layer. These vias are ideally thru-vias (i.e., penetrate all the way through the PCB), and must be plated. The content on this webpage is protected by copyright laws of the United States and of foreign countries. If space does not permit the use of larger vias, then three transition vias of smaller diameter should be used. A variant of the stripline, for PCBs with unequal layer thicknesses (end view). APP 5100: TUTORIALS 5100, AN5100, AN 5100, APP5100, Appnote5100, Appnote 5100 maxim_web:en/products/power/display-power-control/display-drivers,maxim_web:en/products/comms/wireless-rf The choice of bypass capabilities should be made on the basis of the total response of the RF IC frequency, and the expected nature of the frequency distribution of any digital noise of clocks and PLLs. These lines should also be separated from any RF lines that transmit large amounts of RF power. Care must be taken to avoid the coupling not intention between the signal lines. A larger decoupling capacitor (dozens of UFDs) is mounted on the "root" of the star, and smaller capacitors on each of the star branches. The recommended practice is to use a solid soil (container) in layer 2, assuming layer 1 is used for components and rf transmission lines. The return currents induced in the upper layer are short for the underlying layer. If possible, the routes must be filled with the thermally conductive paste to improve the heat sink (the folder is applied after the plating and before the final plate of the plate). For more information, select a wireless or RF product. The smaller value capacitors usually have higher SRFs (for example, a value of 0.2pf in a 0402 SMT packet with an SRF = 14GHz), while the larger values are lower SRFS (for example, a 2PF value in the same package with A SRF = 4GHz). Many of the Maxim RF components require controlled impedance transmission lines that transport RF power to (or) IC pins in PCB. In other words: Bend Radius â € œ3 Â ° â € ™ (width of the line). An array of 5 Âƒ-5 of holes embedded in the central ground plane directly under the RF IC. This is the appropriate method for RF routing in internal layers. The layers assigned to the system system (DC supply) and the soil should be considered in terms of the return current for the components. It should be used in conjunction with all other design and manufacturing guidelines that can be applied to specific components, mu mu me sadazinagro res medop o£Ã§Ãatnemila ed sator sa ,otnemicenrof ed seµÃxenoc sair¡Âv revit etnenopmoc mu eS .lev¡Ãcilpa emrofnoc siairetam ed sotnujnoc e BCP ed Configuration. These transmission lines can be implemented in an outer (upper or lower) layer, or buried in an internal layer. Coplanar Wave Guide (grounded) A CoLopar wave guide provides better insulation between retime RF lines, as well as other signal lines (final view). A typical arrangement is represented in table 2. More detailed image (PDF, 2MB) Figure 9. The material is organized by thematic areas and provides guidance on the "best practices". Alternatively, in some cases, the digital noise can be converted up / down. The route width, the thickness of the dielectric layer and the type of dielectric determine the characteristic impedance (typically 50 Â © or 75 Â ©). The ground plans should not be broken under the routing of the transmission line. For example, the NUCLE FR4 is usually given as ~ tr = 4.2, while the outer layers of the laminate (proprodder) are typically ãžâ µr = 3.8. Examples given below for reference, metal thickness assumed for 1oz of copper (1.4 mils, 0.036mm). For example, in a line of 15 thousand microstrip, a diameter route would be used (Di-Metro finished with plate) of 15 thousand to 18 thousand. The digital noise (of clocks, PLLs, etc.) can be coupled to RF signal lines, and these can be modulated in RF carriers. However, this should be compensated to reduce the discontinuity of the impedance caused by the local increase in the effective width of the line that crosses the curve. Featured impediment There are several calculators available to properly adjust the width of the signal conductive line to achieve the target preventance. It is impractical to achieve a better insulation than approximately -45dB between RF lines in small PCBs. High Speed Digital Signal Lines: These lines should be forwarded separately in a different layer of RF signal lines to avoid coupling. Per arap arap sadamac ed sa§ÂnaduM .BCP od FR ed etrap a adot me etnemlarebil sadanoicida res meved sadamac ertne arret ed saiv sA .)1 arugiF(2 adamaC an odil³Às arret ed onalp mu reuqer)roirepus latem(1 adamaC an pirtsorcim mu Lines When layout constraints require a transmission line to move to a different layer, it is recommended that at least two track holes be used for each transition to minimize the track induction load. Figure 13. Stripline suspended (end view). A pair of tracks will effectively cut the transition inductance by 50%, and the largest track diameter should be used that is compatible with the width of the transmission line. The secondary function of this "ground plane" component is to provide a thermal sink, so the plane must include the maximum number of tracks that are allowed by PCB design rules. Microstrip example (isometric view). decoupling from the main power supply). The general guideline is not to have signals routed in layers between the polarization layer and the ground layer.

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